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(71) Applicant: NEC CORPORATION
Tokyo (JP)

(72) Inventors:
- Kusaba, Kazuyuki,
c/o NEC IC Microcomp. Syst. Ltd.
Kawasaki-shi, Kanagawa (JP)
- Iwamoto, Makoto,
c/o NEC IC Microcomp. Syst. Ltd.
Kawasaki-shi, Kanagawa (JP)

(74) Representative: Betten & Resch
Reichenbachstrasse 19
80469 München (DE)

(54) Semiconductor device having a protective wiring layer

(57) A semiconductor device includes a semiconductor chip, a protective wiring layer, and an abnormality detector. At least one of integrated circuits is formed on the semiconductor chip. The protective wiring layer is formed to be spread on the integrated circuit at a very small interval, and made of a conductive light-shielding material. The protective wiring layer is applied with a power supply voltage upon operating the integrated circuit. The abnormality detector monitors the voltage applied to the protective wiring layer and outputs an abnormality detection signal when the monitored voltage is an abnormal voltage.

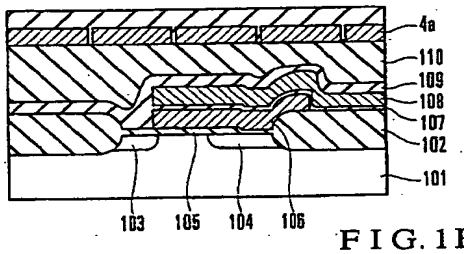

FIG. 1B

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another example of a protective wiring layer;

Fig. 4 is a sectional view showing part of a conventional EEPROM cell; and

Fig. 5 is a plan view of a semiconductor chip showing the state wherein a light-shielding film is formed on a conventional EEPROM.

Description of the Preferred Embodiments

The present invention will be described in detail below with reference to the accompanying drawings.

Fig. 1A schematically shows a semiconductor device according to an embodiment of the present invention. Referring to Fig. 1A, an EEPROM 2 and a random circuit 3 are formed as integrated circuits on a semiconductor chip 1. Conductive light-shielding protective wiring layers 4a and 4b made of Al are respectively formed on the EEPROM 2 and the random circuit 3. The material constituting the protective wiring layers 4a and 4b is not limited to Al, and another conductive light-shielding metal material such as Cu or Ti may also be used.

One end of each of the protective wiring layers 4a and 4b is connected to a power supply VDD, and the other end is connected to ground 6 through a corresponding one of resistors 5a and 5b. The protective wiring layers 4a and 4b have predetermined widths and are formed on the EEPROM 2 and the random circuit 3 such that adjacent wires are spread in a zigzag shape at a very small interval without contacting each other. That is, the protective wiring layers 4a and 4b function as light-shielding films covering predetermined regions corresponding to the EEPROM 2 and the random circuit 3. This structure prevents light from entering a portion below the covered region.

A fault detector 7 is connected to the protective wiring layers 4a and 4b between the EEPROM 2 and the resistor 5a and between the random circuit 3 and the resistor 5b. A fault state memory unit 8 is connected to the fault detector 7 to store an output from the fault detector 7.

Fig. 1B shows the main part of the EEPROM 2 in Fig. 1A. Referring to Fig. 1B, a source 103 and a drain 104 are formed at a predetermined interval in a region defined by a field oxide film 102 on a p-type semiconductor substrate 101. A floating gate 106 electrically insulated from surroundings is formed through a gate insulating film 105 on the semiconductor substrate and the drain between the source 103 and the drain 104. A control gate 108 is formed on the floating gate 106 and the field oxide film 102 through an insulating film 107.

The floating gate 106 and the control gate 108 are made of heavily doped polysilicon. The protective wiring layer 4a shown in Fig. 1B is formed on the semiconductor substrate 101 including the control electrode 108 through interlevel insulating films 109 and 110. The protective wiring layer 4a is formed to have a small interval determined by the interlevel insulating film 110 so as to prevent adjacent interconnections from contacting each other.

In the above structure, part of the gate insulating film 105 between the floating gate 106 and the drain 104 is formed as thin as about 10 nm. In a data erase, when the control gate 108 is applied with a positive voltage much higher than a voltage to the drain 104, electrons enter the floating gate 106 from the drain 104 in the region of the thin gate insulating film 105. In a data write, by changing the polarity of the voltage applied to the control gate 108, the electrons within the floating gate 106 are removed to the drain 104.

During the operation of the semiconductor device, a power supply voltage VDD is kept applied to the protective wiring layers 4a and 4b, and the potentials of the protective wiring layers 4a and 4b are kept at potentials (normal potentials) defined by the resistors 5a and 5b. When the light-shielding film is damaged, i.e., the protective wiring layer 4a is disconnected, the potential between the disconnected portion of the protective wiring layer 4a and the resistor 5a changes to an abnormal potential different from the normal potential. Similarly, when the protective wiring layer 4b is disconnected, the potential between the disconnected portion of the protective wiring layer 4b and the resistor 5b changes to an abnormal potential different from the normal potential.

The fault detector 7 monitors the potential on one end side of each of the resistors 5a and 5b, and upon detecting the abnormal potential at even one end side, outputs an fault (abnormality) detection signal. The fault detection signal output from the fault detector 7 is stored in the fault state memory unit 8.

According to this embodiment, the protective wiring layers 4a and 4b protect the EEPROM 2 and the random circuit 3 from irradiation of light (ultraviolet rays). Therefore, in, e.g., the EEPROM 2, stored data can be protected from being erased by irradiation of light (ultraviolet rays).

In addition, it can be detected without externally observing the semiconductor device that the protective wiring layer 4a or 4b is damaged, and an abnormality has occurred in stored data by irradiation of light through the damaged portion. That is, if the protective wiring layer 4a or 4b is damaged, a fault detection signal is output from the fault detector 7 and stored in the fault state memory unit 8. By checking the memory contents of the fault state memory unit 8, an abnormality in stored data can be detected.

Fig. 2 shows the fault detector 7 and the fault state memory unit 8.

Referring to Fig. 2, the fault detector 7 is constituted by inverters 71 and 72 for respectively inverting input signals from the protective wiring layers 4a and 4b, and an OR circuit 73 for ORing outputs from the inverters 71 and 72. The fault state memory unit 8 is constituted by a flip-flop 81.

In this arrangement, if the protective wiring layers 4a and 4b are not disconnected, the OR circuit 73

receives two "L"-level inputs. Accordingly, the OR circuit 73 outputs an "L"-level signal, and the flip-flop 81 holds the "L"-level signal. To the contrary, if either of the protective wiring layers 4a and 4b is disconnected, either of two inputs to the OR circuit 73 changes to "H" level. Then, the OR circuit 73 outputs an "H"-level signal, and the flip-flop 81 holds the "H"-level signal.

Whether an output from the flip-flop 81 is at "L" or "H" level is checked, and if it is at "H" level, a data abnormality is confirmed to be generated in the semiconductor device in Fig. 1A.

The semiconductor device in Fig. 1A may be formed not to operate when the output from the flip-flop 81 is at "H" level. Alternatively, as shown in Fig. 2, a reset circuit 9 may be connected to the output stage of the flip-flop 81, and the semiconductor device in Fig. 1A may be initialized when the output from the flip-flop is at "H" level. That is, upon detection of a data abnormality in the semiconductor device, the use of the defective semiconductor device is disabled. With this arrangement, a device incorporating the defective semiconductor device can be prevented from malfunctioning.

The above embodiment has exemplified the case wherein the protective wiring layer constituting the light-shielding film is formed in a zigzag shape. The present invention is not limited to this, and a protective wiring layer 201 may be formed into a rectangular spiral shape, as shown in Fig. 3A. In this case, to connect one end of the protective wiring layer 201 to the power supply, and the other end to the fault detector, the other end 202 of the protective wiring layer must be extracted from the central portion of the protective wiring layer 201 through an insulating film.

As shown in Fig. 3B, a protective wiring layer 203 may be formed in a lattice or reticulate shape with a structure of two wiring layers in directions perpendicular to each other. In this case, the protective wiring layer 203 is obtained by connecting, through a contact 203c, a lower protective wiring layer 203a and a protective wiring layer 203b formed above the lower protective wiring layer 203a through an insulating film. The protective wiring layer 203 can further improve light-shielding properties.

As has been described above, according to the present invention, since the protective wiring layer having light-shielding properties is spread at a very small interval in a predetermined region on a semiconductor chip, the state wherein a data abnormality has occurred by irradiation of light on the integrated circuit owing to the damage to the protective wiring layer can be electrically detected.

Claims

1. A semiconductor device characterized by comprising:

   a semiconductor chip (1) on which at least one integrated circuit (2, 3) is formed;

   a protective wiring layer (4a, 4B, 203, 203) formed to be spread on said integrated circuit at a very small interval, and made of a conductive light-shielding material, said protective wiring layer being applied with a power supply voltage upon operating said integrated circuit; and

   abnormality detecting means (7) for monitoring the voltage applied to said protective wiring layer and outputting an abnormality detection signal when the monitored voltage is an abnormal voltage.

2. A device according to claim 1, further comprising:

   fault state memory means (8) for holding the abnormality detection signal output from said abnormality detecting means and storing a fault state of said integrated circuit.

3. A device according to claim 1, further comprising:

   reset means (9) for stopping an abnormal operation of said integrated circuit in accordance with the abnormality detection signal output from said abnormality detecting means.

4. A device according to claim 1, wherein said protective wiring layer formed on said integrated circuit has one end connected to a power supply and the other end grounded through a resistor, and

   said abnormality detecting means monitors a voltage at a connection point between the other end of said protective wiring layer and said resistor.

5. A device according to claim 1, wherein said protective wiring layer is formed into a zigzag shape on said integrated circuit, and

   zigzag portions of said protective wiring layer are electrically insulated by a small-width insulating film.

6. A device according to claim 1, wherein said protective wiring layer is formed into a spiral shape on said integrated circuit, and

   spiral portions of said protective wiring layer are electrically insulated by a small-width insulating film.

7. A device according to claim 1, wherein said protective wiring layer comprises:

   a lower protective wiring layer (203a) formed

into a zigzag shape in one direction; and

an upper protective wiring layer (203b) formed into a zigzag shape in a direction perpendicular to said lower protective wiring layer, and electrically connected to said lower protective wiring layer through a contact (203c),

zigzag portions of said lower protective wiring layer and zigzag portions of said upper protective wiring layer being electrically insulated by small-width insulating films, and

said lower and upper protective wiring layers being electrically insulated by an insulating film.

8. A device according to claim 1, wherein said integrated circuit is constituted by an electrically erasable programmable read only memory.

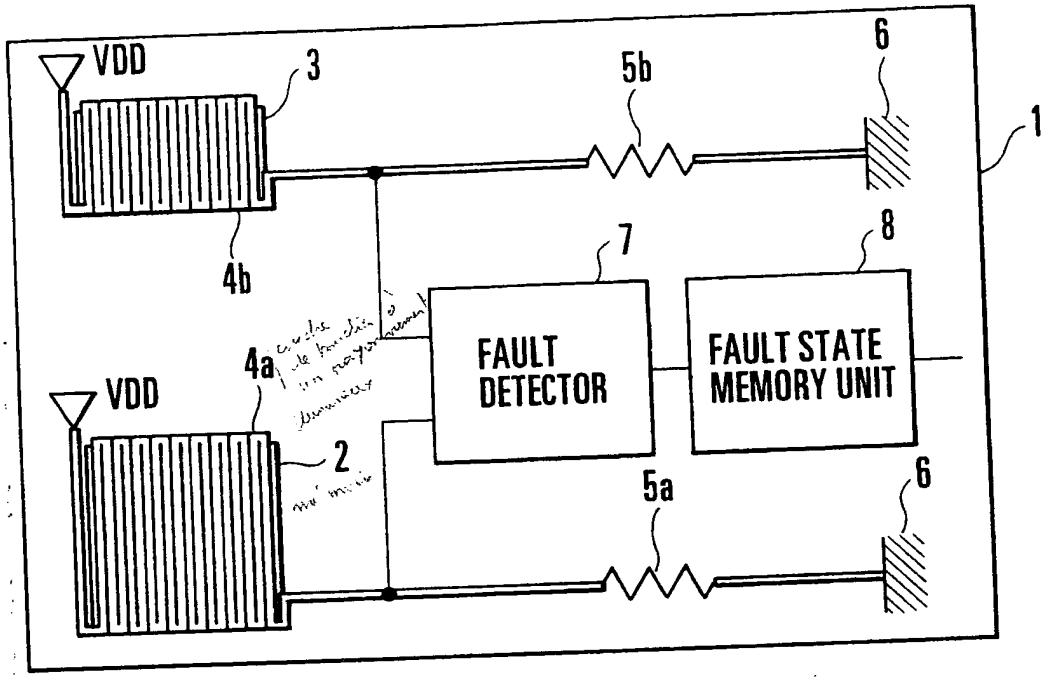
VDD
3
5b
6
1
4b
7
8
FAULT DETECTOR
FAULT STATE MEMORY UNIT
4a
VDD
2
5a
6

FIG. 1A

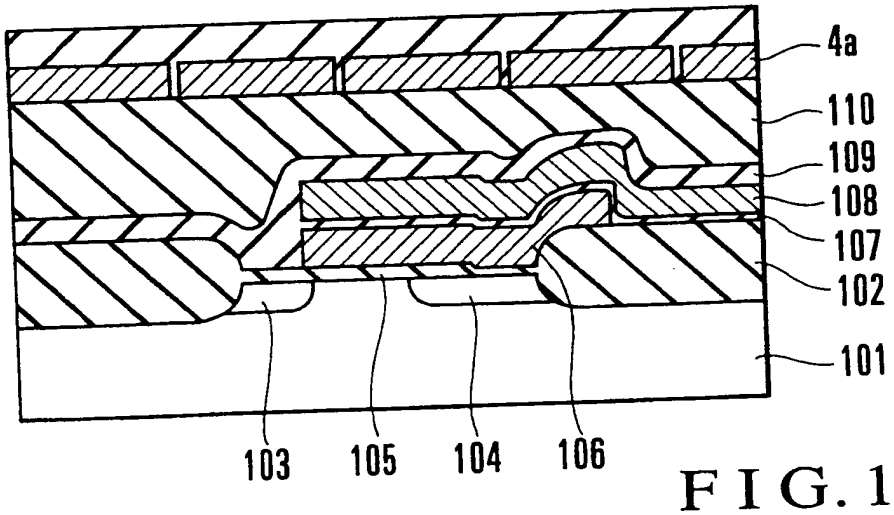
4a
110
109
108
107
102
101
103
105
104
106

FIG. 1B

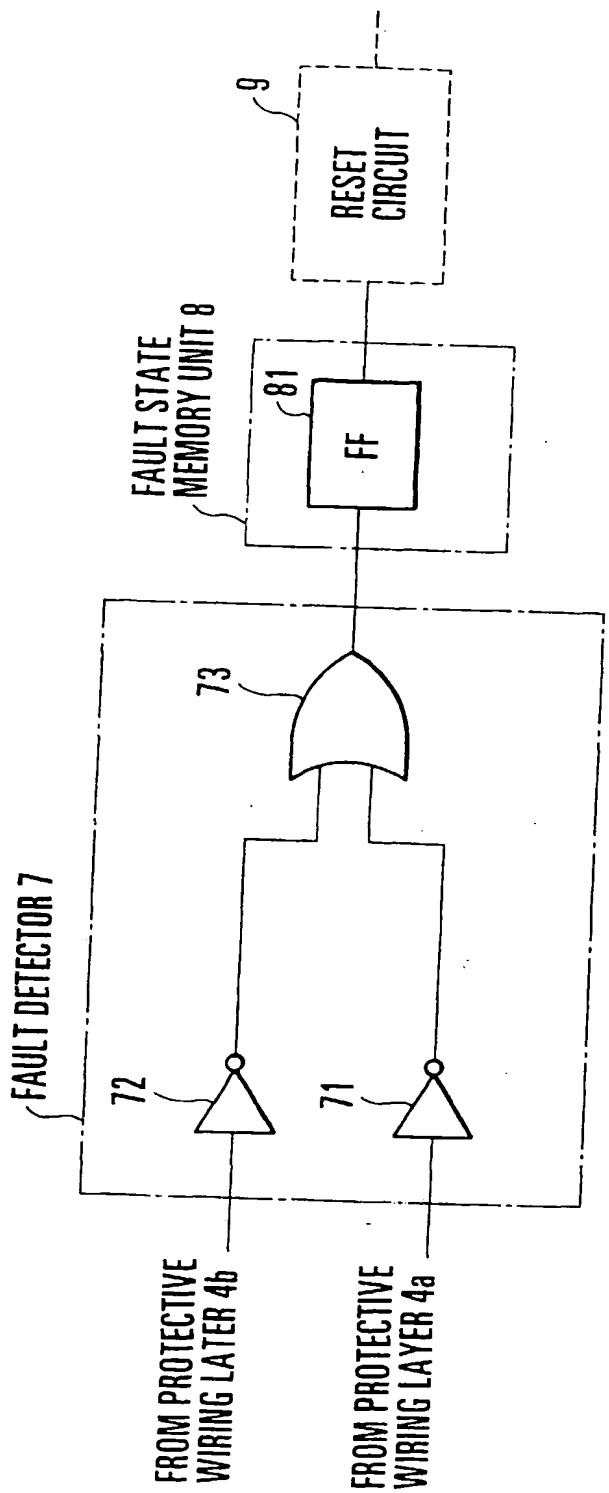

FIG. 2

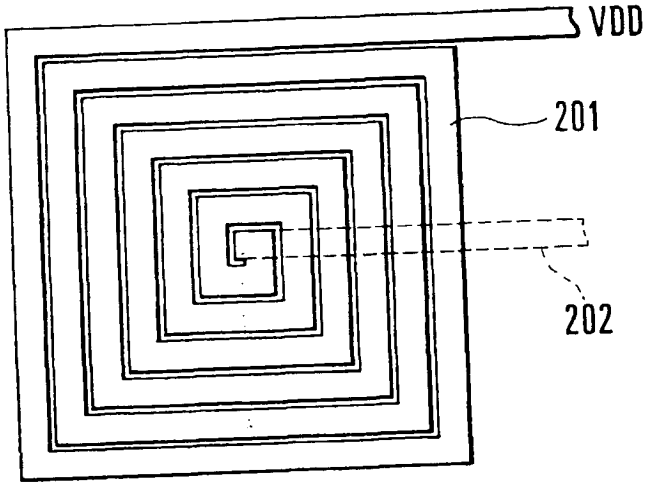

FIG. 3A

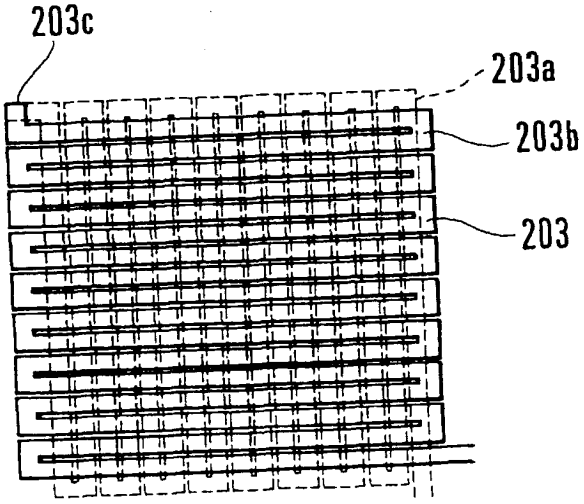

FIG. 3B

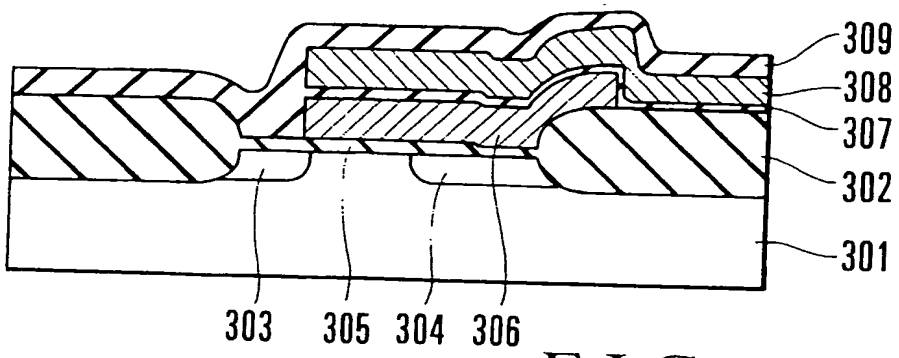

FIG. 4
PRIOR ART

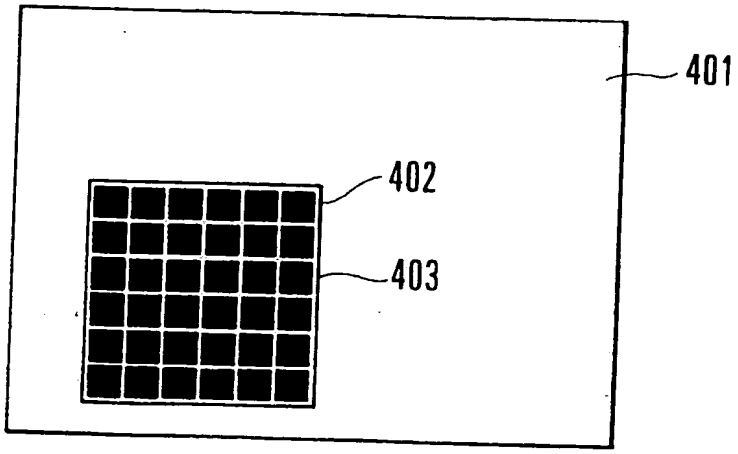

FIG. 5
PRIOR ART

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(72) Inventors:
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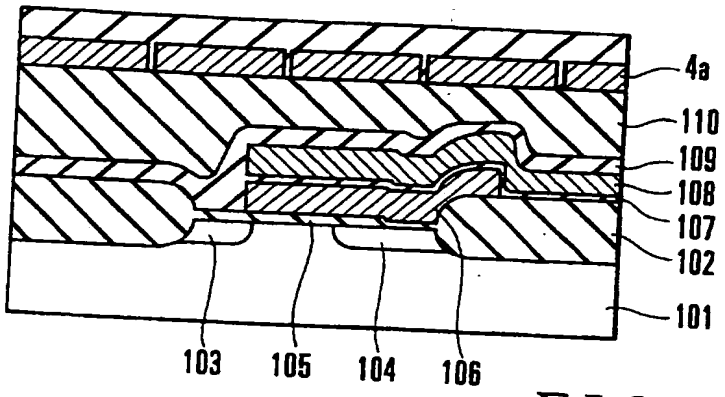

FIG. 1B

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EUROPEAN SEARCH REPORT

Application Number
EP 98 10 7308

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A	US 4 519 050 A (FOLMSBEE ALAN C) 21 May 1985 (1985-05-21) * claims 1,6 *	1,8	
A	EP 0 582 850 A (TEXAS INSTRUMENTS INC) 16 February 1994 (1994-02-16) * claim 1; figure 1B *	1	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)
H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	31 August 1999	De Raeve, R

CATEGORY OF CITED DOCUMENTS

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